What is claimed is :

1. An apparatus for receiving digital motion pictures, comprising:

a video bit stream extracting means for separating and extracting a bit stream including video signals; and

a video display processor for carrying out down-conversion by converting the extracted video stream to a field DCT coded block if the video bit stream is an interlaced scanning sequence with a frame DCT coded block, while carrying out a down-conversion as it is if the video bit stream has a field DCT coded block, and storing the down-conversion result in a memory for motion compensation.

2. An apparatus for receiving digital motion pictures of claim 1, wherein the video display processor performs variable length decoding and interlacing of an input bit stream and performs 4x4 inverse discrete cosine transform IDCT after removing a DCT coefficient of a high frequency component in horizontal/vertical directions if the DCT coefficient is a field DCT type of an interlaced sequence, while performs a downsampling in a vertical direction in a converted field DCT domain after removing the DCT coefficient of the high frequency component in the horizontal direction and converting to a field DCT data if the DCT coefficient is a frame DCT type.

3. An apparatus for receiving digital motion pictures of claim 1, wherein, the video display processor performs up-sampling filtering in vertical/horizontal directions with relation to a data read from the memory before the motion compensation in case that full resolution motion vectors are utilized for the motion compensation, and performs down-sampling filtering in the vertical/horizontal directions after the motion compensation.

4. A video decoding device in which input video bit streams are restored into

pixel values of an original screen by the steps of inverse quantization IQ after variable length decoding VLD, inverse discrete cosine conversion IDCT, and motion compensation MC, comprising:

a down-sampling IDCT part for carrying out 4X4 inverse discrete cosine transform IDCT after removing DCT coefficients of high frequency components in horizontal/vertical directions if the inverse quantized DCT coefficient are field DCT coded data, while performs down-sampling of a frame DCT coded data in vertical direction in a DCT domain after removing DCT coefficients of the high frequency components in horizontal direction to convert it to field DCT coded data if the inverse quantized DCT coefficients are the frame DCT coded data;

a memory for storing the IDCT data of an IDCT part or a result of adding the IDCT data to motion compensated data;

an up-sampling part for carrying out up-sampling of a reference picture which is read from a memory in horizontal/vertical directions;

a motion compensation part for carrying out motion compensation with relation to the picture which is up-sampled in horizontal/vertical directions in the up-sampling part by using motion vectors of a variable length decoded full resolution;

a down-sampling part for carrying out down-sampling of the motion-compensated data in the motion compensation part in horizontal/vertical directions and storing in the memory after adding to the IDCT data; and

a video display processor for reading the data stored in the memory according to a display mode to output to a display device.

5. A video decoding device of claim 4, wherein the IDCT part comprises:

a horizontal reduction part for removing the DCT coefficients of the high

frequency components in horizontal direction if an input data is the frame DCT coded block of the interlaced sequence;

a frame/field converter for converting the frame DCT coded block, of which DCT coefficients of the high frequency components in the horizontal direction are removed, to the field DCT coded block;

a matrix multiplier for down-sampling the field DCT coded block in the vertical direction to output the IDCT coefficients of a field structure; and

a horizontal IDCT for carrying out IDCT in the horizontal direction with relation to the output data from the matrix multiplier.

6. A video decoding device of claim 4, wherein the frame/field converter converts two vertical blocks [x] having eight frame DCT coefficients to two field DCT coded blocks [Xtb] with relation to top and bottom fields by applying following matrix

$$[Xtb] = [T_f][IT8_2][X] = \begin{bmatrix} \begin{bmatrix} Xt \\ Xt \\ Xt \\ Xt \\ Xt \\ Xt \\ Xt \\ Xt \end{bmatrix} \\ \begin{bmatrix} Xb \\ Xb \\ Xb \\ Xb \\ Xb \\ Xb \\ Xb \\ Xb \end{bmatrix} \end{bmatrix}$$

wherein,

$$T_f = \begin{bmatrix} \rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow \\ t_0 \; 0 \; t_1 \; 0 \; t_2 \; 0 \; t_3 \; 0 \; t_4 \; 0 \; t_5 \; 0 \; t_6 \; 0 \; t_7 \; 0 \\ \rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow \\ 0 \; t_0 \; 0 \; t_1 \; 0 \; t_2 \; 0 \; t_3 \; 0 \; t_4 \; 0 \; t_5 \; 0 \; t_6 \; 0 \; t_7 \end{bmatrix}$$

$$[IT8_2] = \begin{bmatrix} T8^T & 0 \\ 0 & T8^T \end{bmatrix}$$

[T8] represent 8x8 DCT basis matrix consisting of 8-point DCT bases, IDCT with relation to two vertical blocks are represented by [$IT8_2$] matrix, and $\vec{t_i}$ represents i-th 8-point DCT basis vectors.

7. A video decoding device of claim 5, wherein the matrix multiplier outputs IDCT coefficients [ytb] of field units which are down-sampled in the horizontal/vertical direction by applying following matrix.

$$[ytb] = [Q][X] = [IP4_2][T_f][IT8_2][X] = \begin{bmatrix} yt \\ yt \\ yt \\ yt \\ yb \\ yb \\ yb \\ yb \end{bmatrix}$$

wherein,

$[IP4_2] = \begin{bmatrix} T4^T 00 \;\; 0 \\ 0 \;\; 00T4^T \end{bmatrix} / \sqrt{2}$ is a down-sampling matrix of field DCT coded coefficients, and [T4] represents 4x4 DCT matrix consisting of 4-point DCT bases,

$$T_f = \begin{bmatrix} \rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow \\ t_0 \; 0 \; t_1 \; 0 \; t_2 \; 0 \; t_3 \; 0 \; t_4 \; 0 \; t_5 \; 0 \; t_6 \; 0 \; t_7 \; 0 \\ \rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow\rightarrow \\ 0 \; t_0 \; 0 \; t_1 \; 0 \; t_2 \; 0 \; t_3 \; 0 \; t_4 \; 0 \; t_5 \; 0 \; t_6 \; 0 \; t_7 \end{bmatrix}$$

$$[IT8_2] = \begin{bmatrix} T8^t & 0 \\ 0 & T8^t \end{bmatrix}$$

wherein, [T8] represents 8x8 DCT basis matrix consisting of 8-point DCT bases, IDCT for two vertical blocks is represented by $[IT8_2]$ matrix, $\vec{t_i}$ represents i-th 8-point DCT basis vectors, and [X] represents two vertical blocks having eight frame DCT coefficients.

8. A video decoding device of claim 7, wherein the matrix [Q] of the matrix multiplier is 8x16 matrix which operates only for the DCT coefficients in the vertical direction.

9. A video decoding device of claim 4, wherein the up-sampling part selects fields proper for the motion vectors in case of the motion compensation, and carries out the up-sampling filtering in the horizontal/vertical directions for the respective fields after reading reference blocks corresponding to the selected fields from the memory.

10. A video decoding device of claim 4, wherein the motion compensation part forms motion compensated field blocks by half-pel interpolation with relation to the up-sampled blocks in case of the motion compensation using the field prediction, while forms motion compensated frame blocks by the half-pel interpolation after forming reference blocks of the frame units with the up-sampled blocks of the respective fields in case of the motion compensation using the frame prediction, so that the motion compensated frame blocks are separated per the respective fields.

11. A video decoding device of claim 4, wherein the down-sampling part converts eight pixels into four pixels by applying following 4x8-dimensional down-sampling matrix C_{4x8}.

$$C_{4\times 8} = C_4^T \cdot T_8$$

wherein, $C_4 = \begin{bmatrix} T_4 \\ 0 \end{bmatrix} / \sqrt{2}\,C$ and T_8 represents a matrix consisting of 8x8 DCT bases, and T_4 represents a matrix consisting of 4x4 DCT bases.

12. A video decoding device of claim 4, wherein the up-sampling part converts four pixels to eight pixels by applying following up-sampling matrix.

$$2 \cdot C_{4\times8}^{T}$$

13. A video decoding device of claim 4, wherein the video display processor further includes a post-processing filter for amending the bottom fields before displaying the reference pictures having the field-based vertical structure on a screen.

14. An apparatus for receiving digital motion pictures, comprising:

a video bit stream extracting means for separating and extracting a bit stream including video signals; and

a video processor for carrying out down-conversion of a DCT coded block and a field DCT coded block to a picture of a pixel structure based on a top field to store in a memory for carrying out motion compensation, if the extracted video bit stream is an interlaced sequence.

15. An apparatus of claim 14, wherein the video display processor performs variable length decoding and inverse quantization for an input video bit stream and removes DCT coefficients of the bottom fields if the inverse-quantized DCT coefficients are the field DCT data of interlaced sequence, and a DCT coefficients of high frequency components of the top field, so as to carry out 8x4 inverse discrete cosine transform, wherein the video display processor removes the DCT coefficients of the high frequency components in the horizontal direction and extracts only the top fields to carry out the IDCT in case of the frame DCT data.

16. An apparatus of claim 14, wherein the video display processor carries out the up-sampling in the horizontal direction by reading the reference data of the top fields from the memory before the motion compensation in case of the motion compensation using full-resolution motion vectors, and the down-sampling in the horizontal direction after the motion compensation.

17. A video decoding device in which input video bit streams are restored into pixel values of an original screen by the steps of inverse quantization IQ after variable length decoding VLD, inverse discrete cosine conversion IDCT, and motion compensation MC, comprising:

an IDCT part for carrying out 8X4 IDCT after removing DCT coefficients of bottom fields and DCT coefficients of high frequency components of top fields if the inverse-quantized DCT coefficients are field DCT data of interlaced sequence, while removing DCT coefficients of high frequency components in horizontal direction and extracting top fields only if the inverse-quantized DCT coefficients are frame DCT data;

a memory for storing the IDCT data of an IDCT part or a result of adding the IDCT data to motion compensated data;

an up-sampling part for carrying out up-sampling of a reference picture which is read from the memory in horizontal direction;

a motion compensation part for carrying out motion compensation with relation to the picture which is up-sampled in horizontal direction in the up-sampling part by using motion vectors of VLD full-resolution;

a down-sampling part for carrying out down-sampling for the data of which motion is compensated in the motion compensation part in horizontal direction and storing in the memory after adding to the IDCT data; and

a video display processor for reading the data stored in the memory according to a display mode to output to a display device.

18. A video decoding device of claim 17, wherein the IDCT part comprises:

a horizontal reduction part for removing the DCT coefficients of the high frequency components in horizontal direction if an input data is a frame DCT coded block of the interlaced sequence;

a converter for converting the frame DCT coded block, of which DCT coefficients of the high frequency components are reduced in the horizontal direction, to the field DCT coded block so as to output IDCT coefficients of the top fields only; and

a horizontal IDCT for carrying out IDCT in the horizontal direction with relation to the output data from the converter.

19. A video decoding device of claim 18, wherein the converter converts the vertical blocks [x] having eight frame DCT coefficients to IDCT coefficients [Xt] of the top fields by applying following matrix.

$$[Xt] = \begin{bmatrix} xt \\ xt \\ xt \\ xt \end{bmatrix} = [Q'][X]$$

$$\text{wherein, } [Q'] = \begin{bmatrix} t_{00}\, t_{10}\, t_{20}\, t_{30}\, t_{40}\, t_{50}\, t_{60}\, t_{70} \\ t_{02}\, t_{12}\, t_{22}\, t_{32}\, t_{42}\, t_{52}\, t_{62}\, t_{72} \\ t_{04}\, t_{14}\, t_{24}\, t_{34}\, t_{44}\, t_{54}\, t_{64}\, t_{74} \\ t_{06}\, t_{16}\, t_{26}\, t_{36}\, t_{46}\, t_{56}\, t_{66}\, t_{76} \end{bmatrix}$$

20. A video decoding device of claim 17, wherein the up-sampling part selects the top fields with relation to the motion vectors of which reference fields are the bottom fields when performing the motion compensation and carries out the up-sampling filtering in the horizontal direction for the selected top field reference signals

in the horizontal direction.

21. A video decoding device of claim 17, wherein the motion compensation part forms motion compensated field blocks by half-pel interpolation using the full-resolution motion vectors with relation to the up-sampled blocks in case of the motion compensation using the field prediction, while forms motion compensated frame blocks by the half-pel interpolation using the full-resolution motion vectors with relation to the up-sampled blocks of the top fields in case of the motion compensation using the frame prediction.

22. A video decoding device of claim 17, wherein the down-sampling part converts eight pixels to four pixels by applying 4x8-dimensional down-sampling matrix C_{4x8}.

$$C_{4\times 8} = P_4^T \cdot T_8$$

wherein, $P_4 = \begin{bmatrix} T_4 \\ 0 \end{bmatrix} / \sqrt{2}$ C and T_8 represents a matrix consisting of 8x8 DCT bases, and T_4 represents a matrix consisting of 4x4 DCT bases.

23. A video decoding device of claim 17, wherein the up-sampling part converts four pixels to eight pixels by applying following up-sampling matrix.

$$2 \cdot C_{4\times 8}^T$$